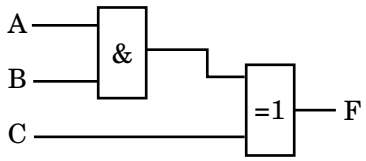
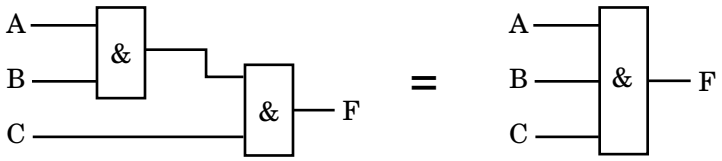
Hoofdstuk 4

Digitale techniek

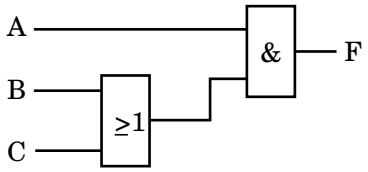


Figuur 4.1: Combinatorische schakeling.

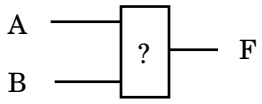
Computersystemen en embedded systemen (LvM)



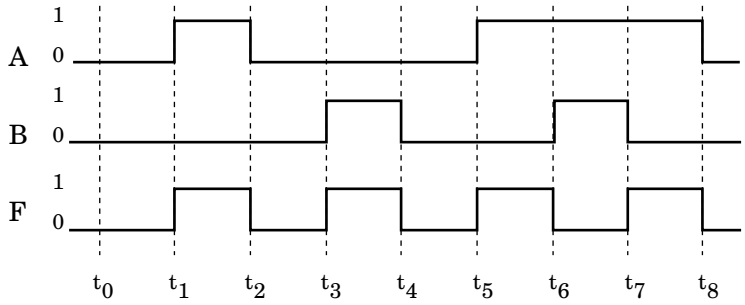
Figuur 4.2: Drie-input AND.



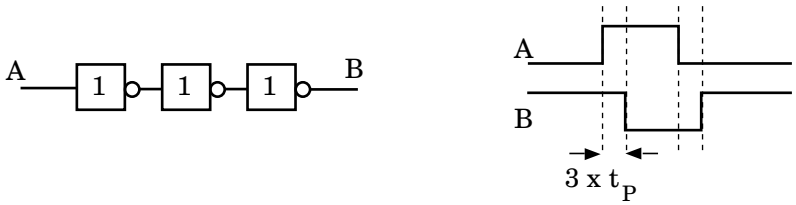
Figuur 4.3: Don't care voorbeeld



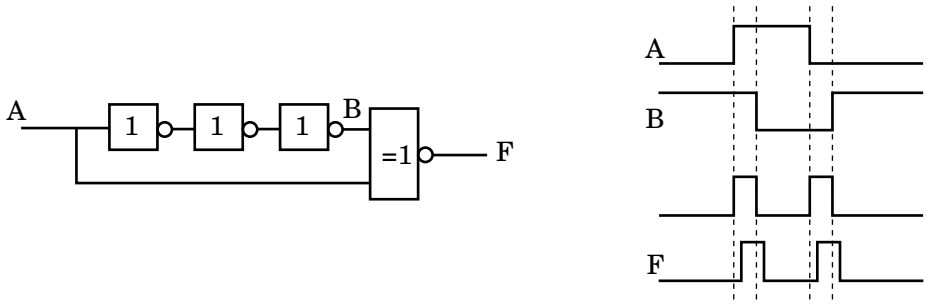
Figuur 4.4: Onbekende logische schakeling.



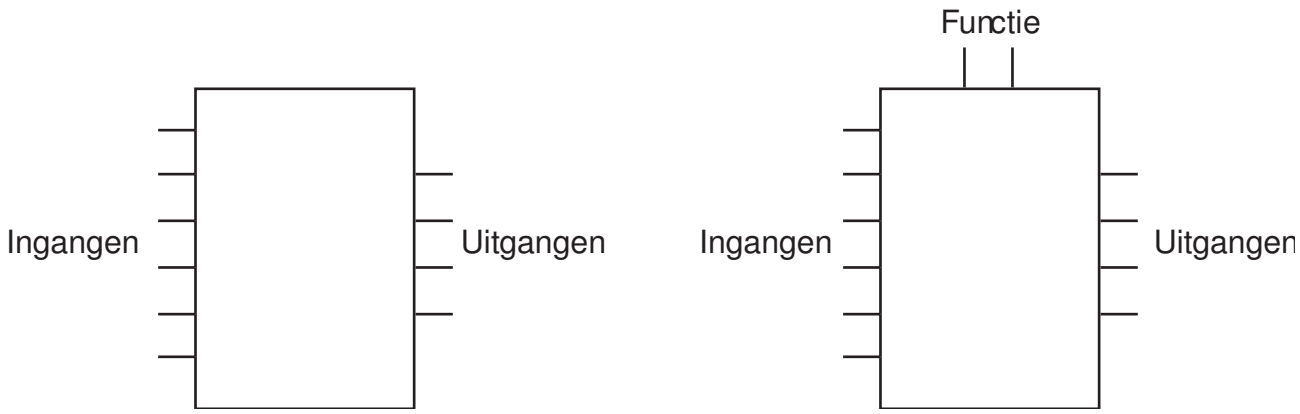
Figuur 4.5: Tijdsdiagram.



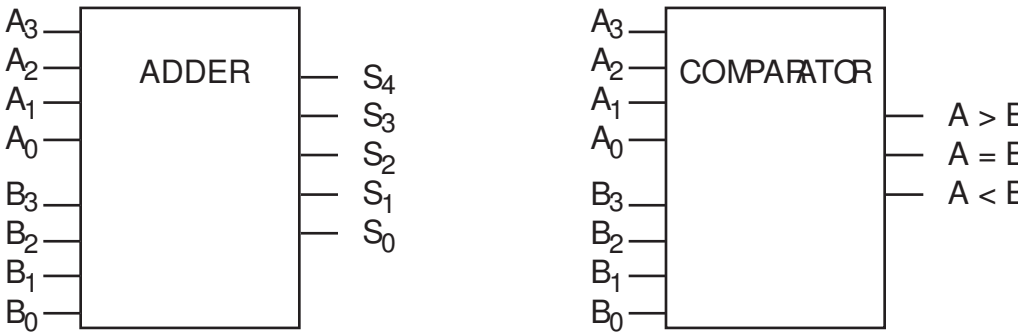
Figuur 4.6: Propagation delay van drie invertors.



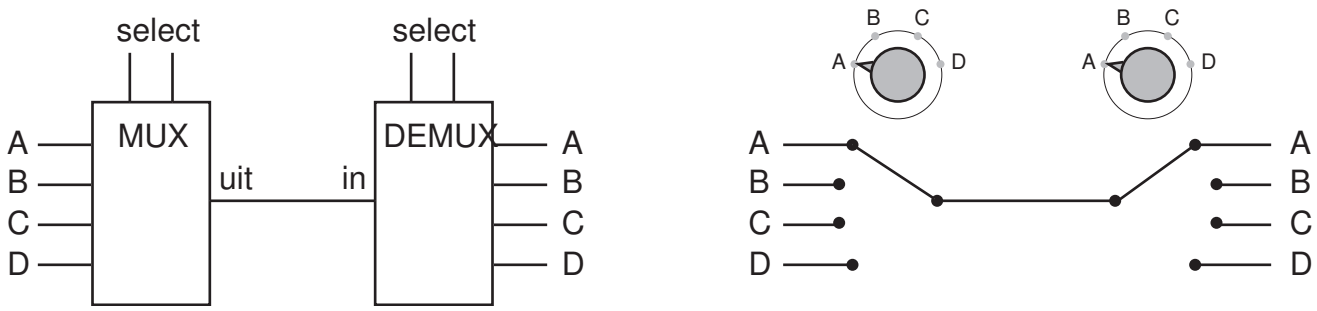
Figuur 4.7: Schakeling met glitches in het tijdsdiagram.



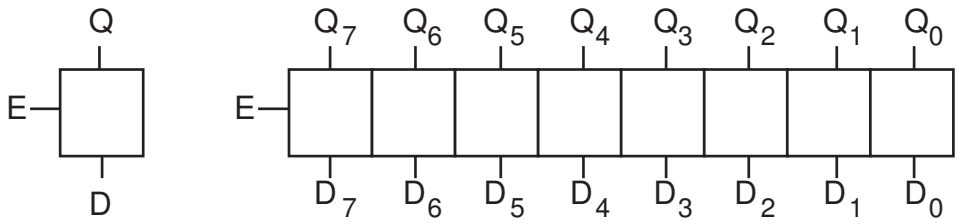
Figuur 4.8: Combinatorische schakelingen.



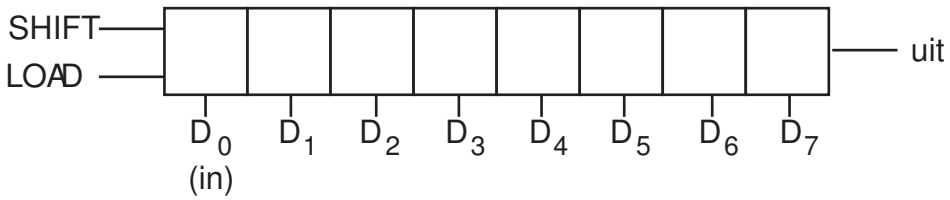
Figuur 4.9: Adder en comparator.



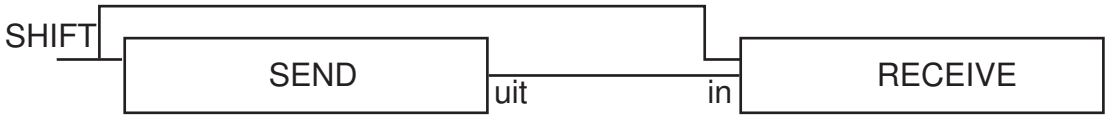
Figuur 4.10: Multiplexer en demultiplexer.



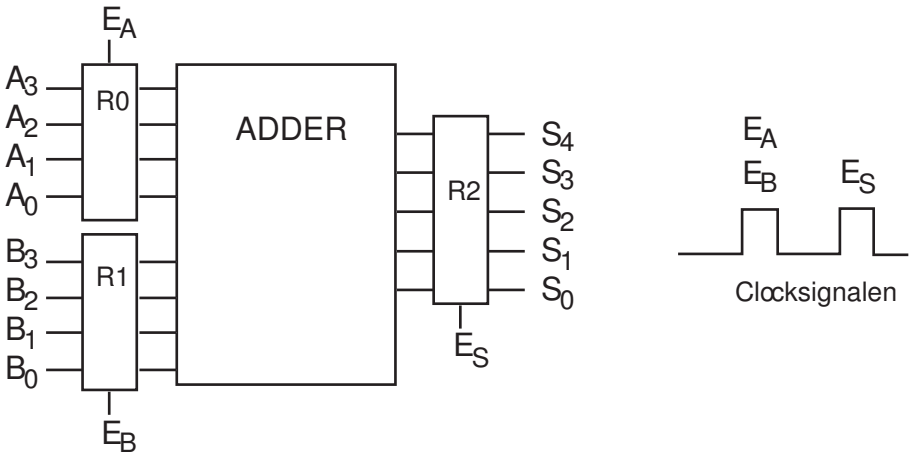
Figuur 4.11: 1-bits en 8-bits geheugenschakeling of register.



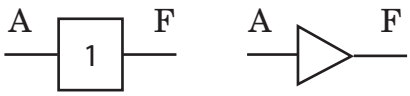
Figuur 4.12: 8-bits schuifregister.



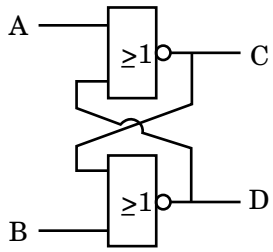
Figuur 4.13: Datatransport met twee schuifregisters.



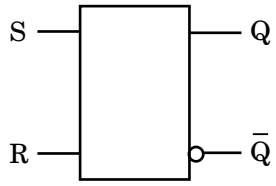
Figuur 4.14: Adder met geheugenelementen.



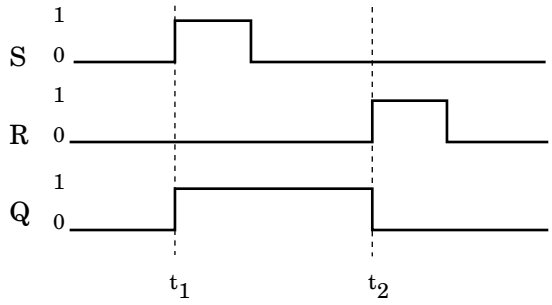
Figuur 4.15: Buffersymbolen.



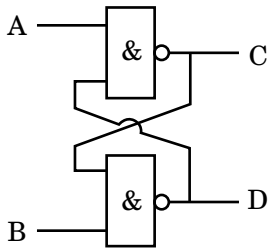
Figuur 4.16: Flipflop met NOR-gates.



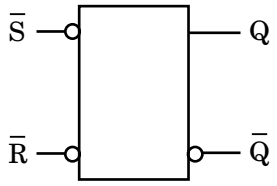
Figuur 4.17: Symboolvan een RS-flipflop.



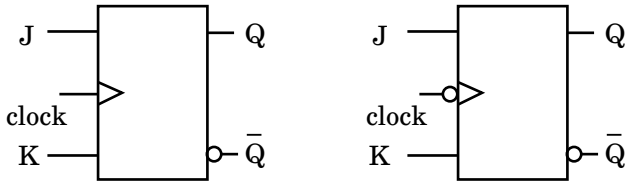
Figuur 4.18: Tijdsdiagram van een RS-flipflop.



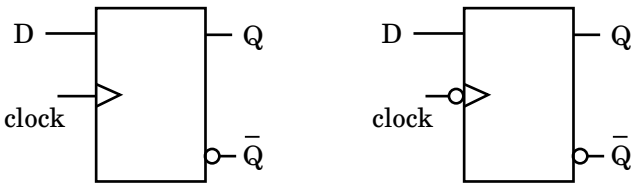
Figuur 4.19: Flipflop mat NAND-gates.



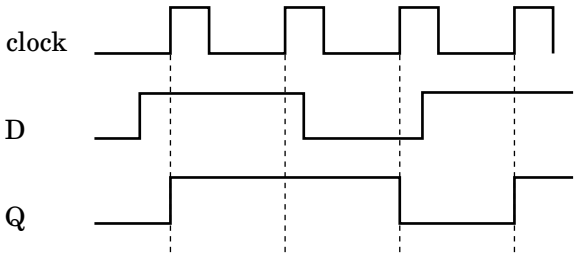
Figuur 4.20: Symbool $\overline{R}\,\overline{S}$ flipflop met active low inputs.



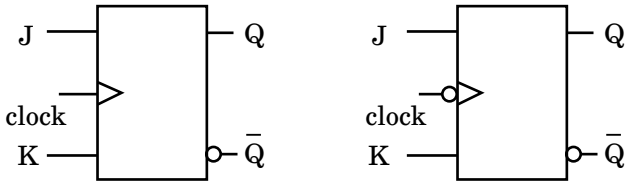
Figuur 4.21: Positieve (links) en negatieve (rechts) flanktriggering.



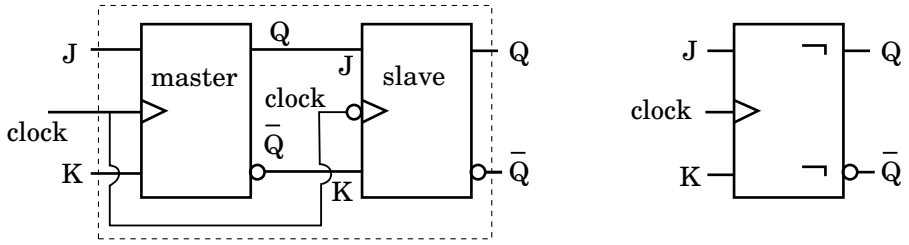
Figuur 4.22: Symbolen D-flipflop.



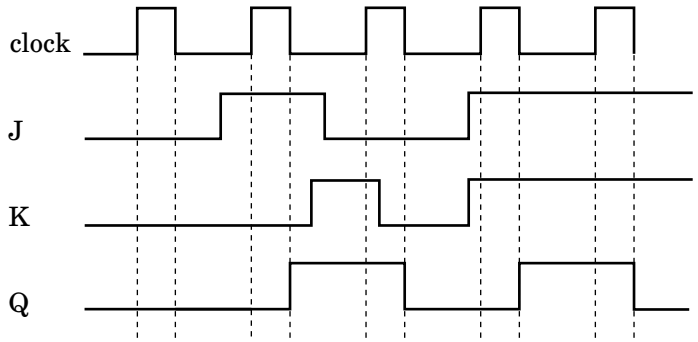
Figuur 4.23: Tijdsdiagram D-flipflop.



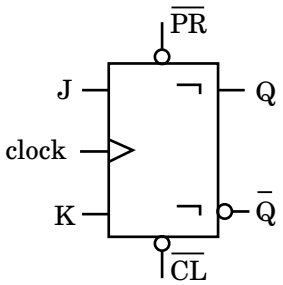
Figuur 4.24: JK-flipflop.



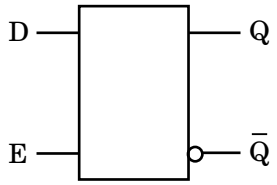
Figuur 4.25: Interne opbouw en symbool van een JK-MS-flipflop.



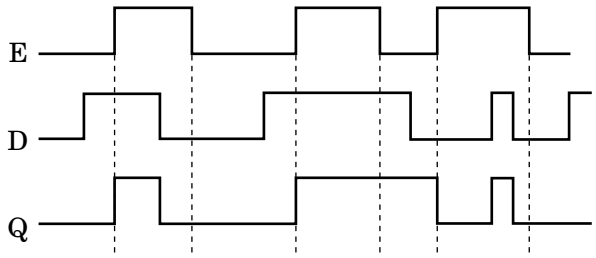
Figuur 4.26: Tijdsdiagram van een JK-master-slave-flipflop.



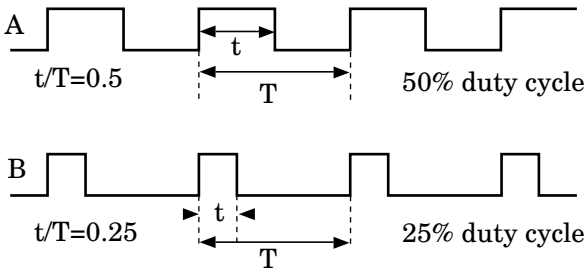
Figuur 4.27: JK-MS-flipflop met preset en clear.



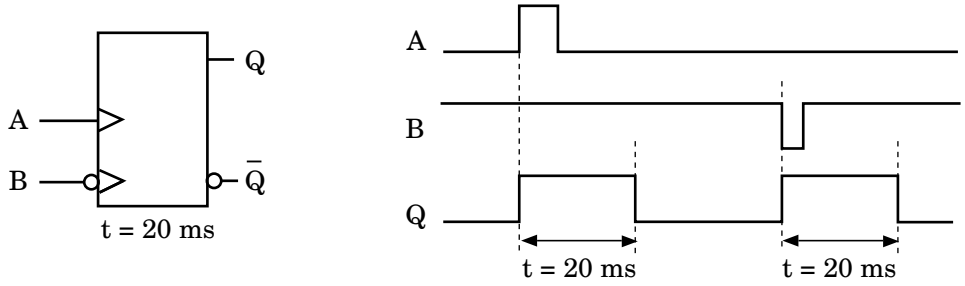
Figuur 4.28: Symbool D-latch.



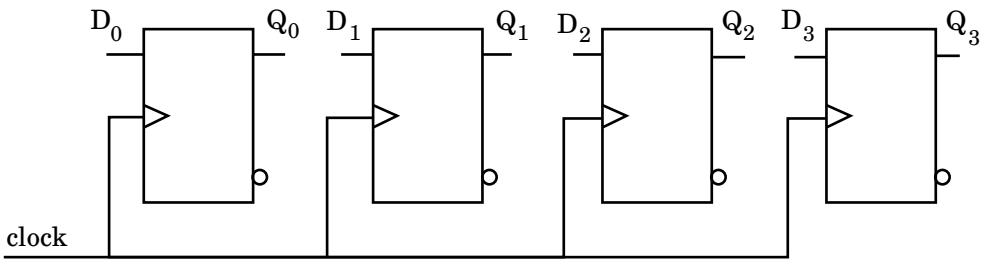
Figuur 4.29: Tijdsdiagram D-latch.



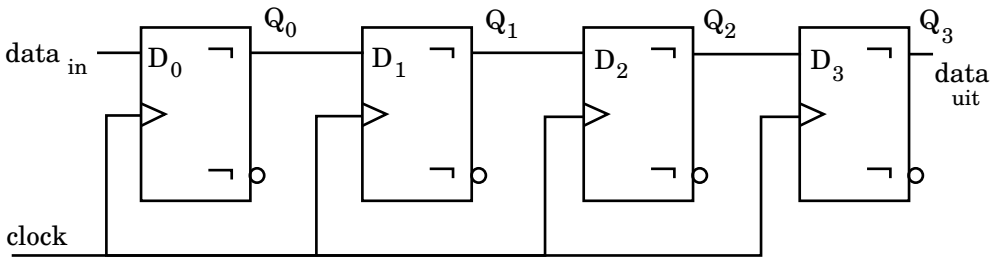
Figuur 4.30: Kloksignalen.



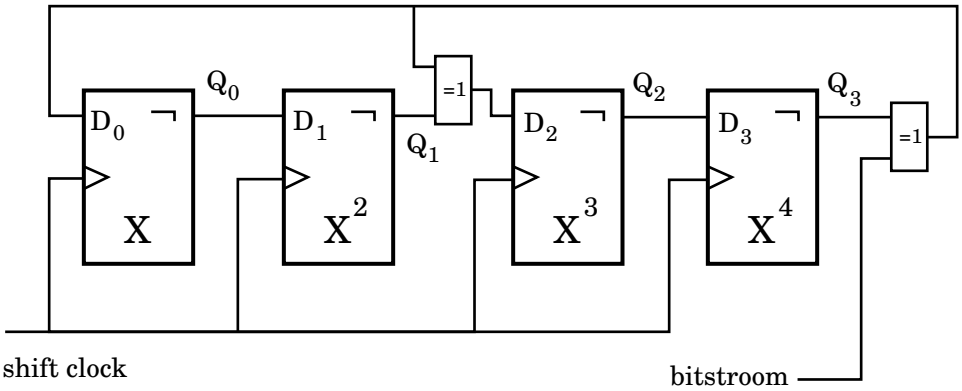
Figuur 4.31: Monostabiele multivibrator.



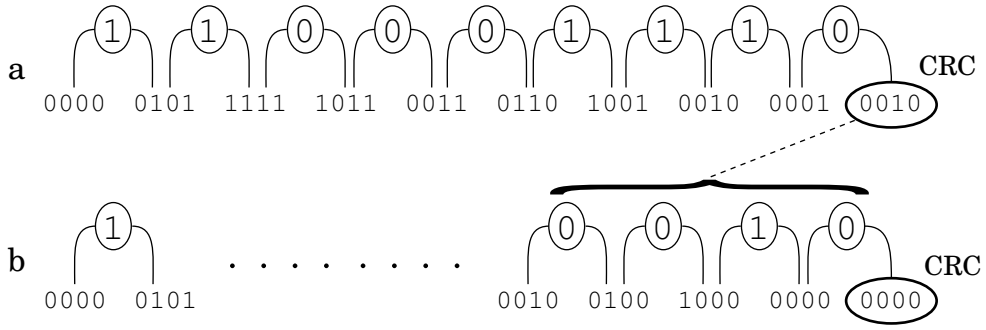
Figuur 4.32: 4-bits register.



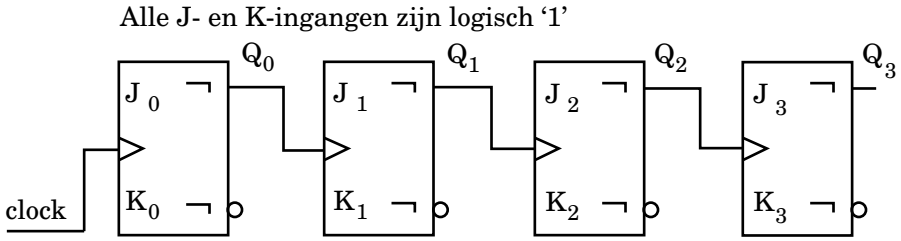
Figuur 4.33: Schuifregister.



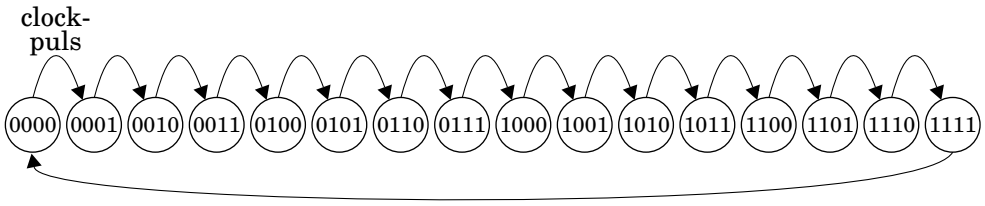
Figuur 4.34: CRC-hardware.



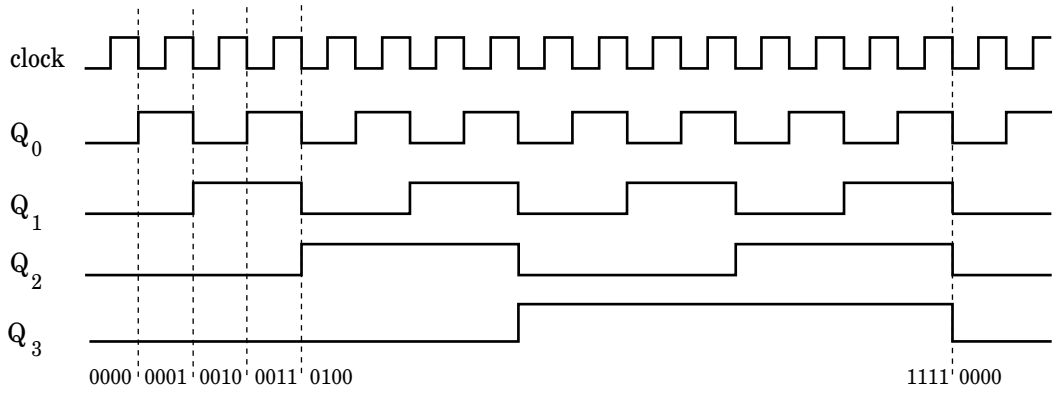
Figuur 4.35: CRC-genereren en CRC controleren.



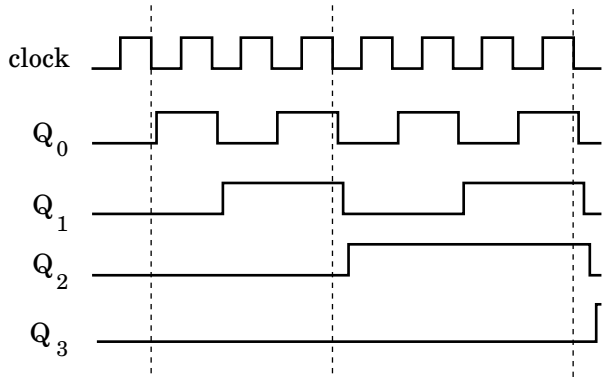
Figuur 4.36: Asynchrone ripple counter.



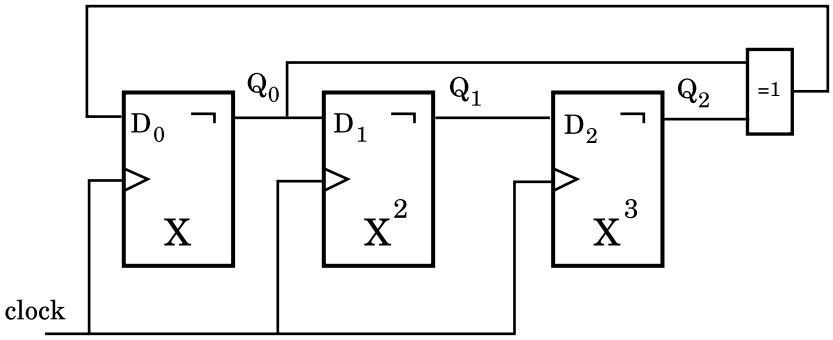
Figuur 4.37: Telsequentie van een 4-bits counter.



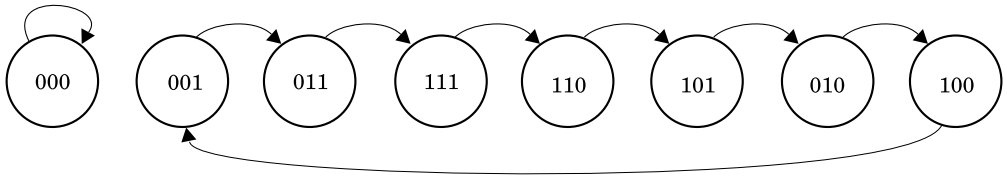
Figuur 4.38: Tijdsdiagram van een ripple counter zonder propagation delay.



Figuur 4.39: Tijdsdiagram van een ripple counter met propagation delay.

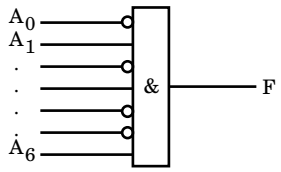


Figuur 4.40: 3-bits pseudo random number generator.

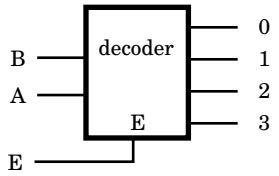


Figuur 4.41: Codesequentie van een 3-bits PRNG.

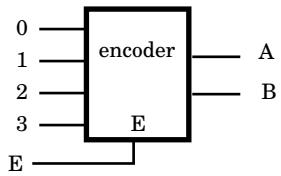
Computersystemen en embedded systemen (LvM)



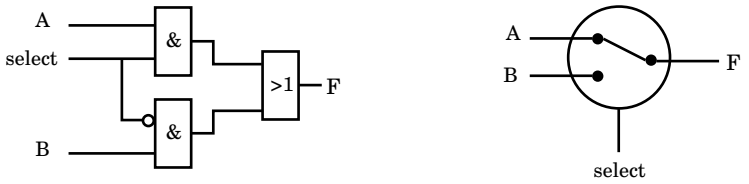
Figuur 4.42: Codedetector.



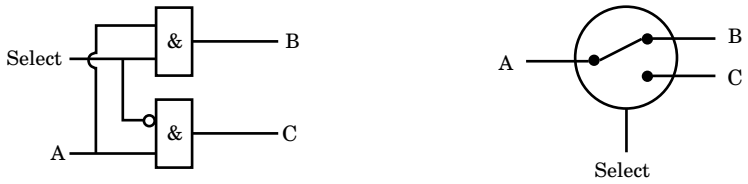
Figuur 4.43: Decoder met enable-ingang.



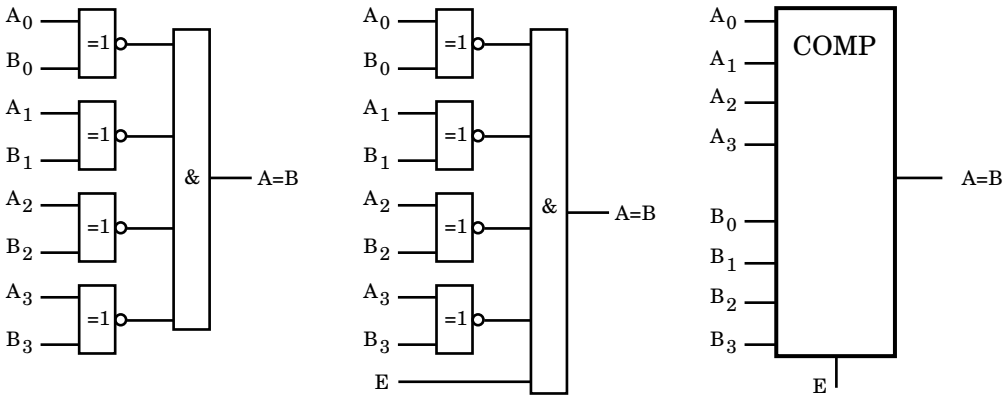
Figuur 4.44: Encoder.



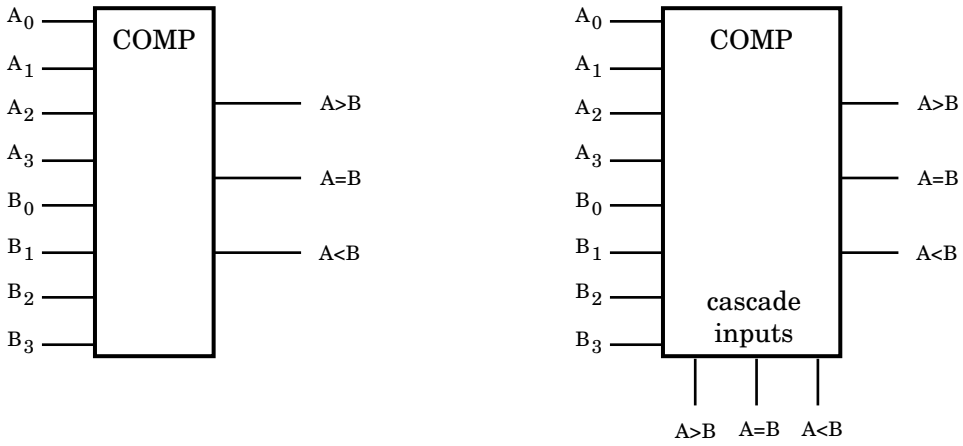
Figuur 4.45: 2-naar-1-multiplexer.



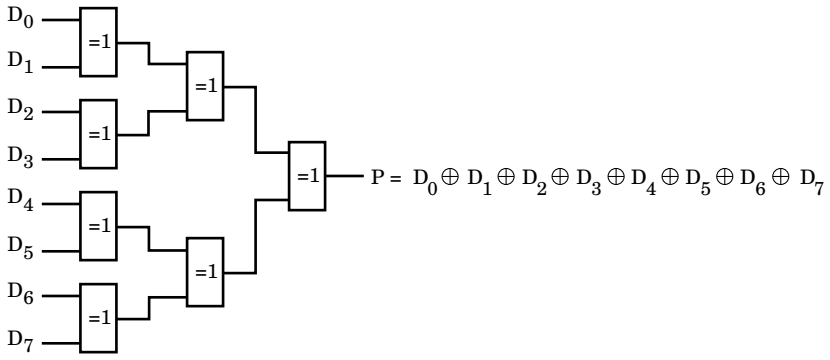
Figuur 4.46: 1-naar-2-demultiplexer.



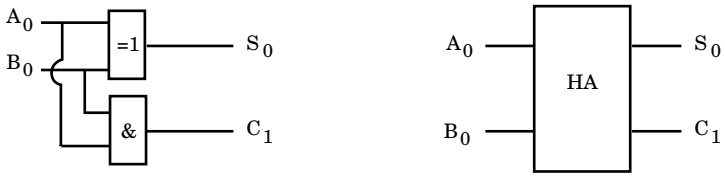
Figuur 4.47: Comparator, realisatie en symbool.



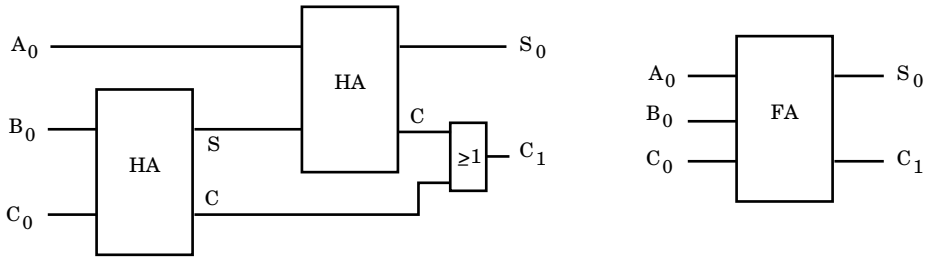
Figuur 4.48: Magnitude comparator.



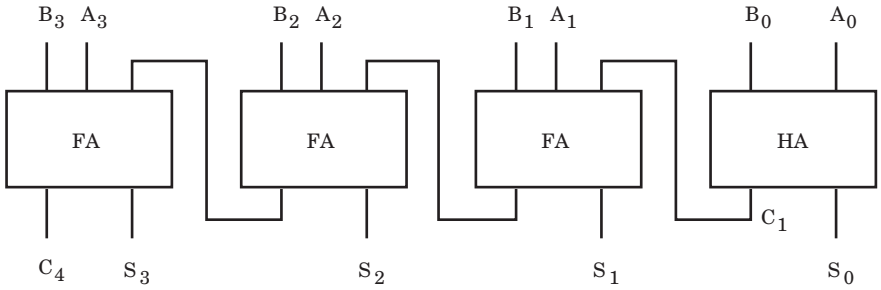
Figuur 4.49: Pariteitsboom.



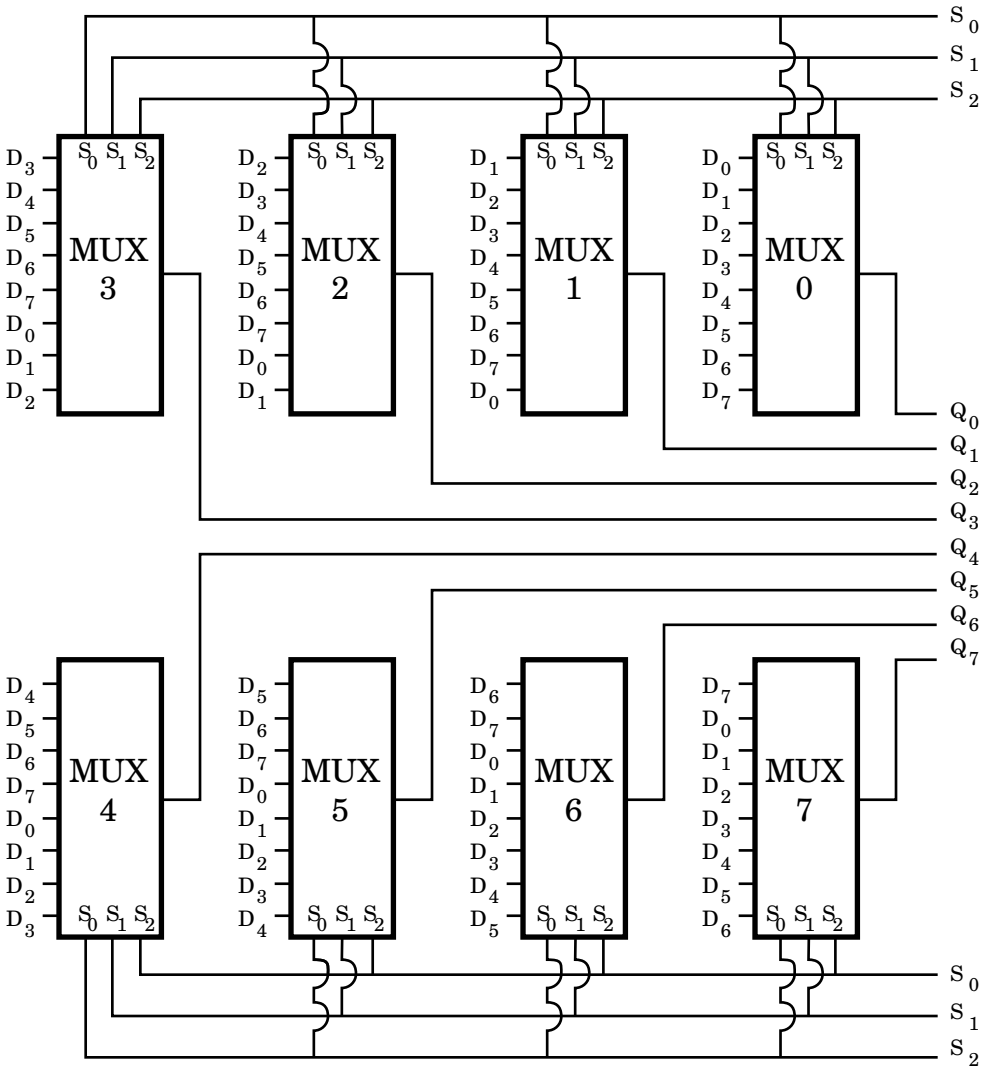
Figuur 4.50: Half adder.



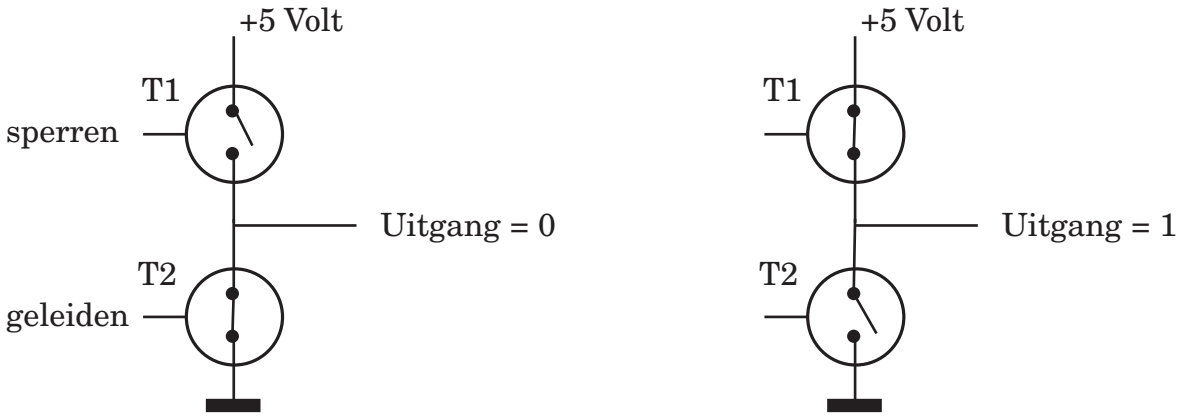
Figuur 4.51: Full adder.



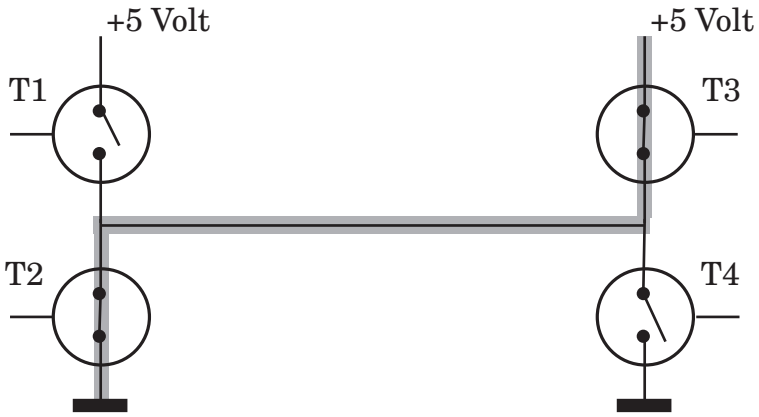
Figuur 4.52: Optelschakeling voor meer bits.



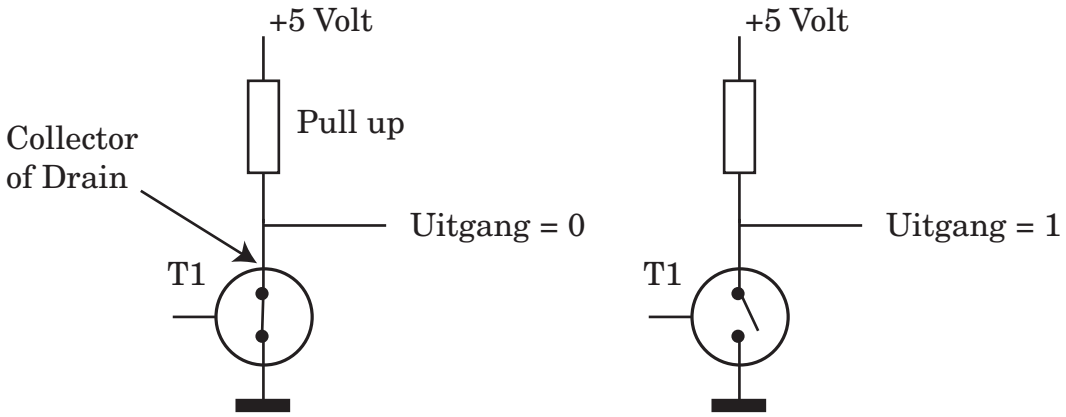
Figuur 4.53: Barrelshufter voor acht bits.



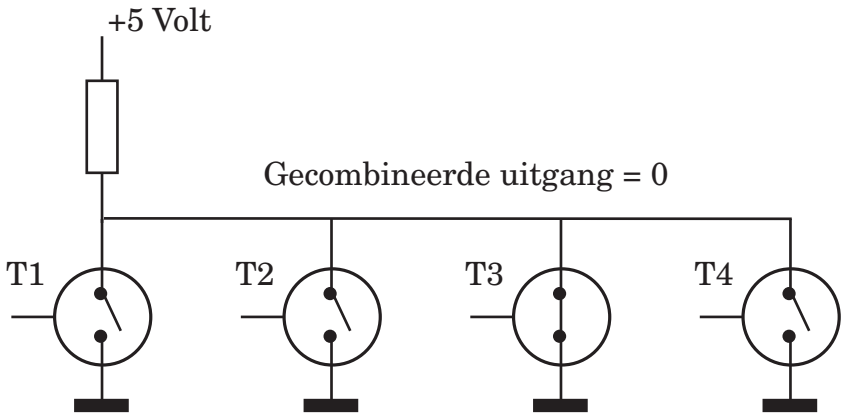
Figuur 4.54: Uitgangen van logische schakelingen.



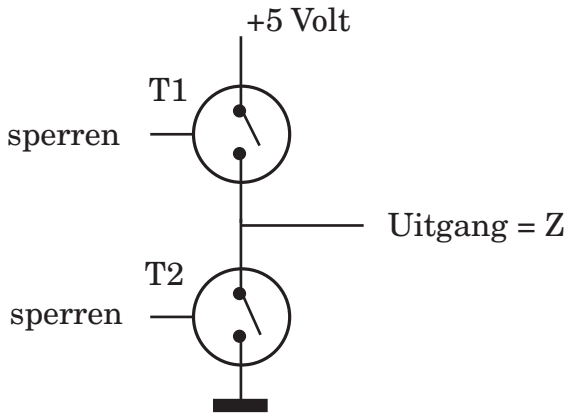
Figuur 4.55: Kortsluiting via T_1 en T_2.



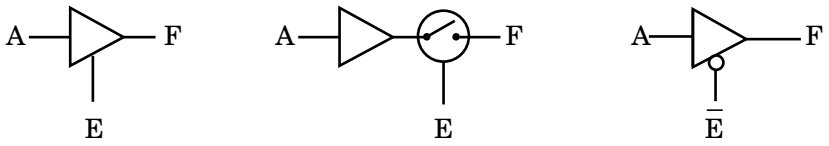
Figuur 4.56: Open collector uitgang met externe pull-up weerstand.



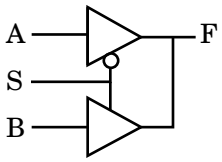
Figuur 4.57: Combinatie van vier uitgangen met één pull-up weerstand.



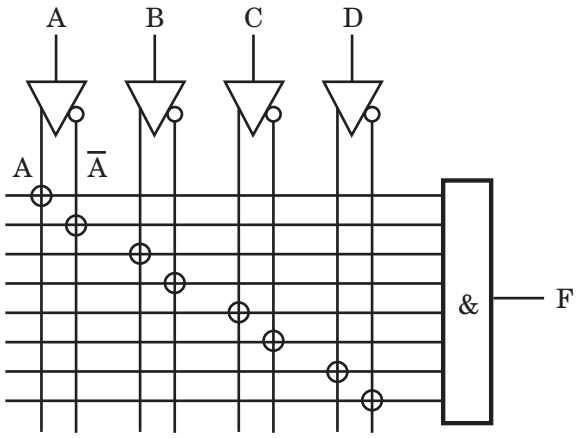
Figuur 4.58: Uitgang in niet-actieve toestand.



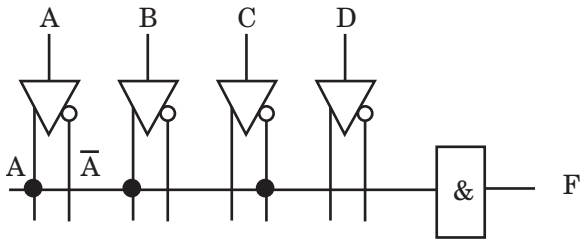
Figuur 4.59: Tristate buffer.



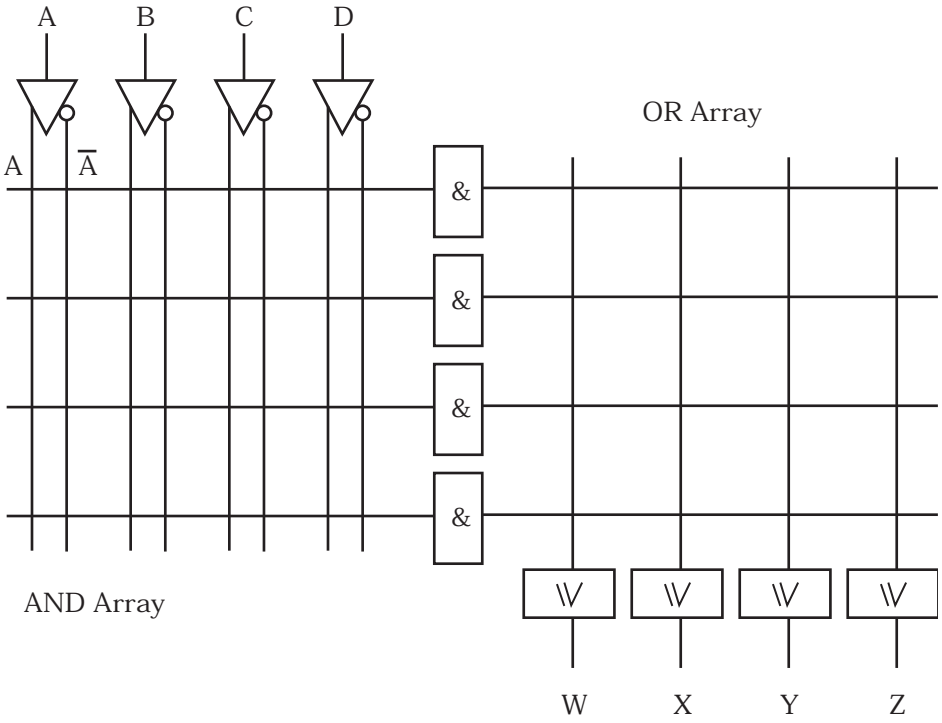
Figuur 4.60: Multiplexer met tristate buffers.



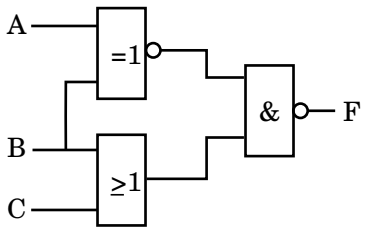
Figuur 4.61: Programmeerbaar array.



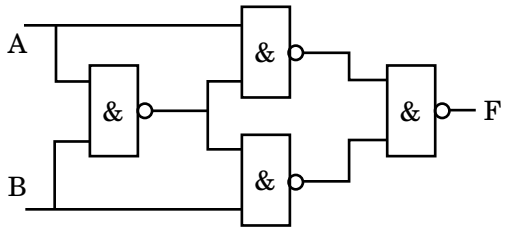
Figuur 4.62: Compacte weergave van een programmeerbaar array.



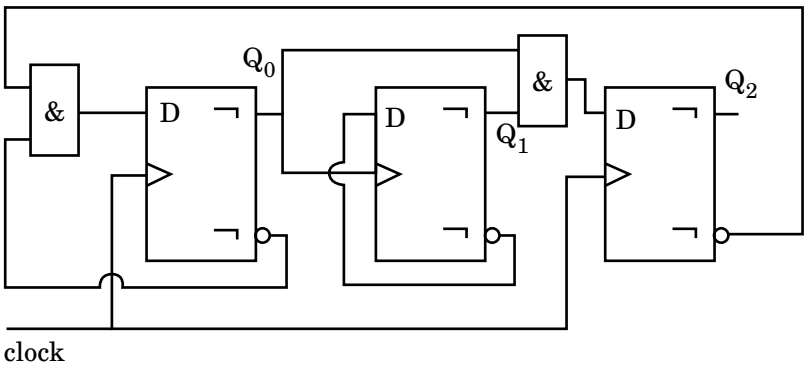
Figuur 4.63: Programmeerbaar AND- en OR-array.



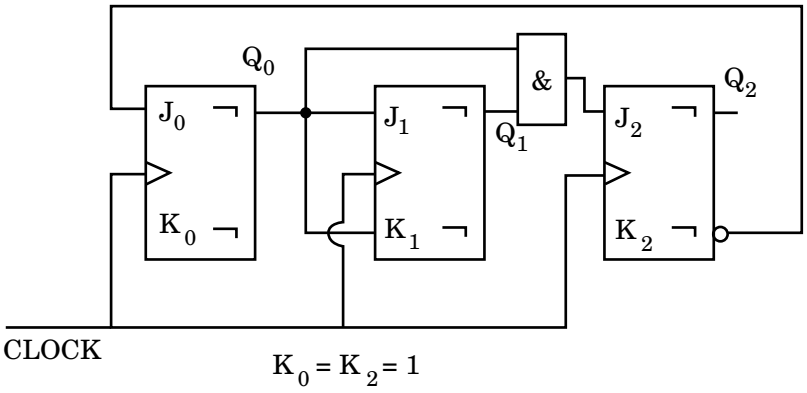
Figuur 4.64: Combinatorische schakeling.



Figuur 4.65: Schakeling met NAND-gates.



Figuur 4.66: Schakeling met D-flipflops.



Figuur 4.67: Schakeling met JK-flipflops.