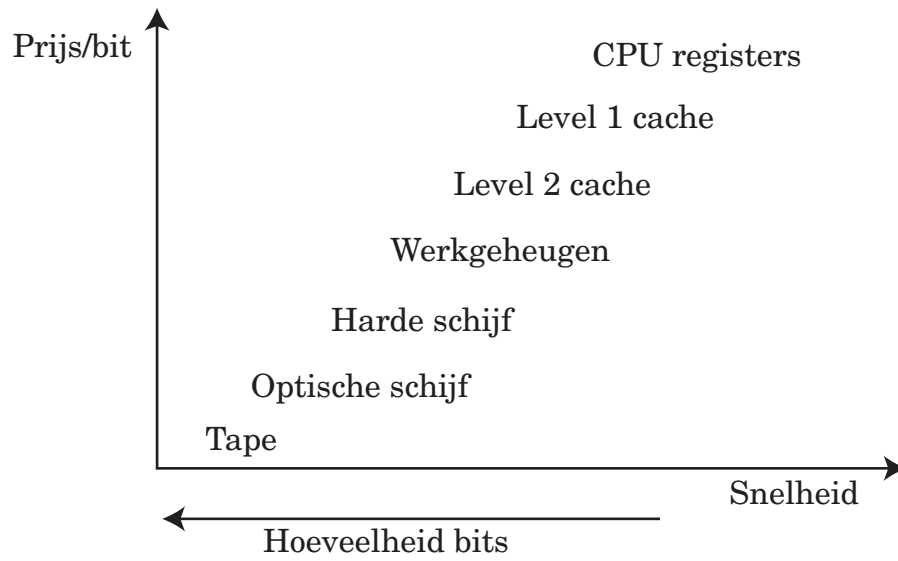


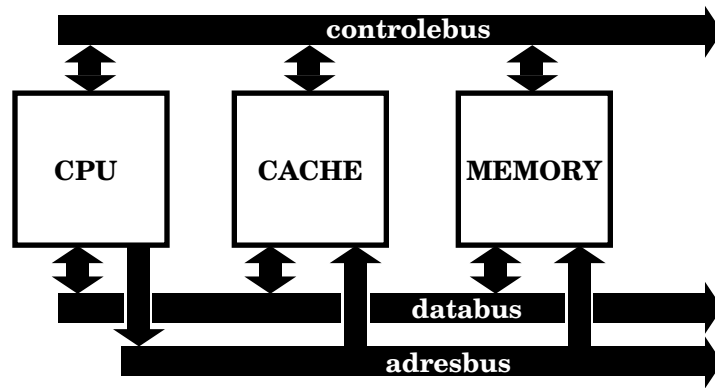
Hoofdstuk 11

Systeemprestatie



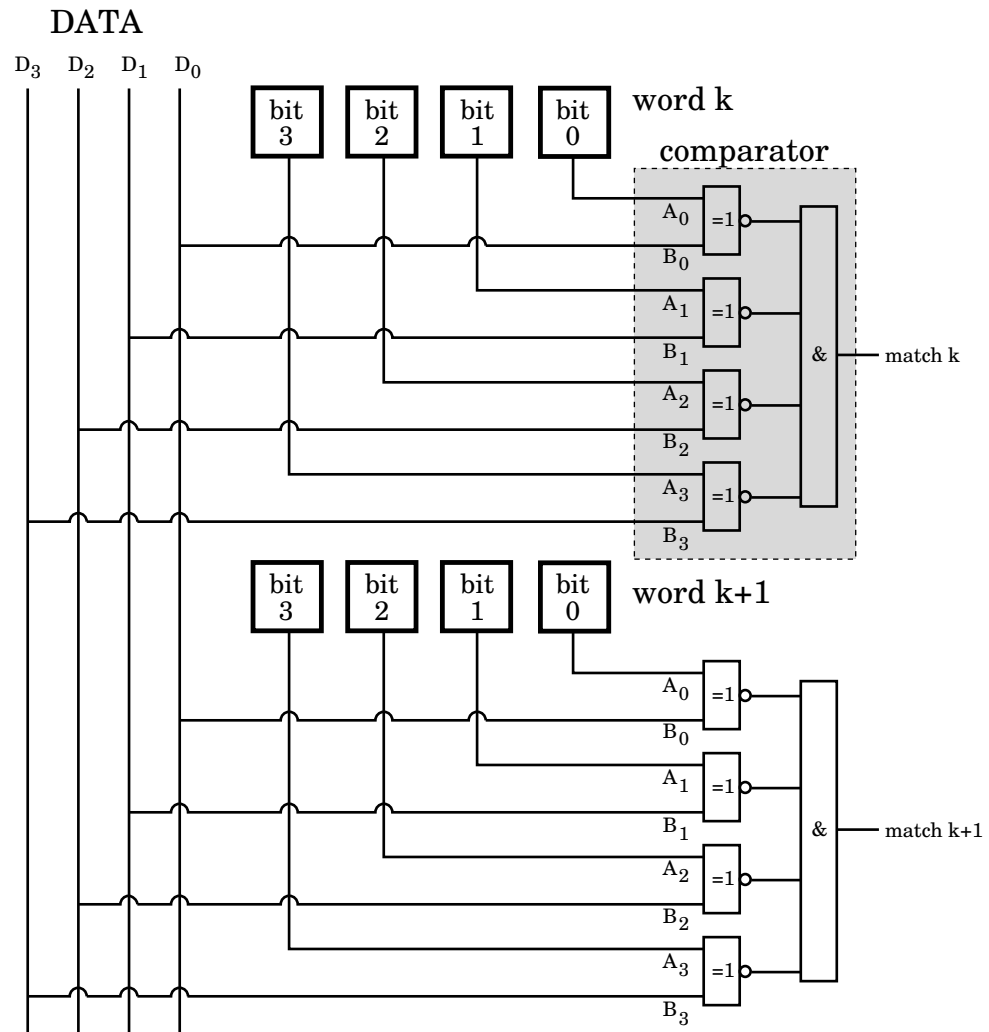
Figuur 11.1: Toegangssnelheid, prijs en hoeveelheid van bits.

Computersystemen en embedded systemen (LvM)

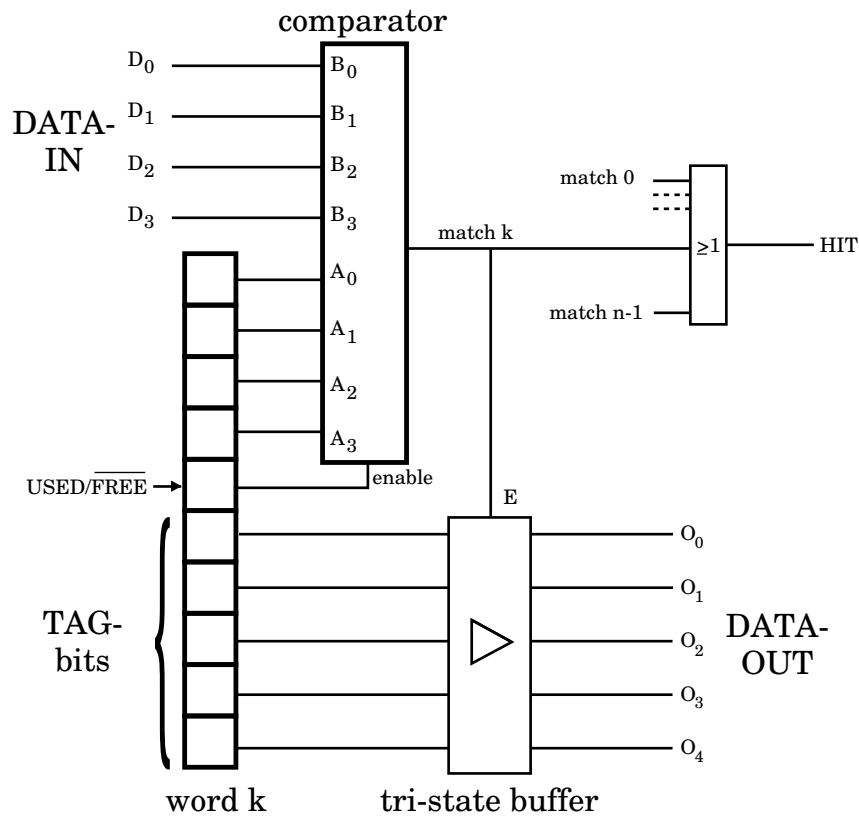


Figuur 11.2: Plaats van de cache in een systeem.

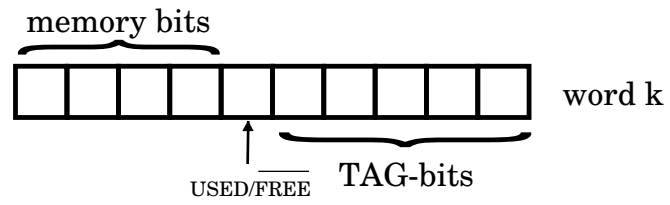
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Figuur 11.3: Organisatie van associatief geheugen.



Figuur 11.4: Geheugenlocatie met TAG-bits.



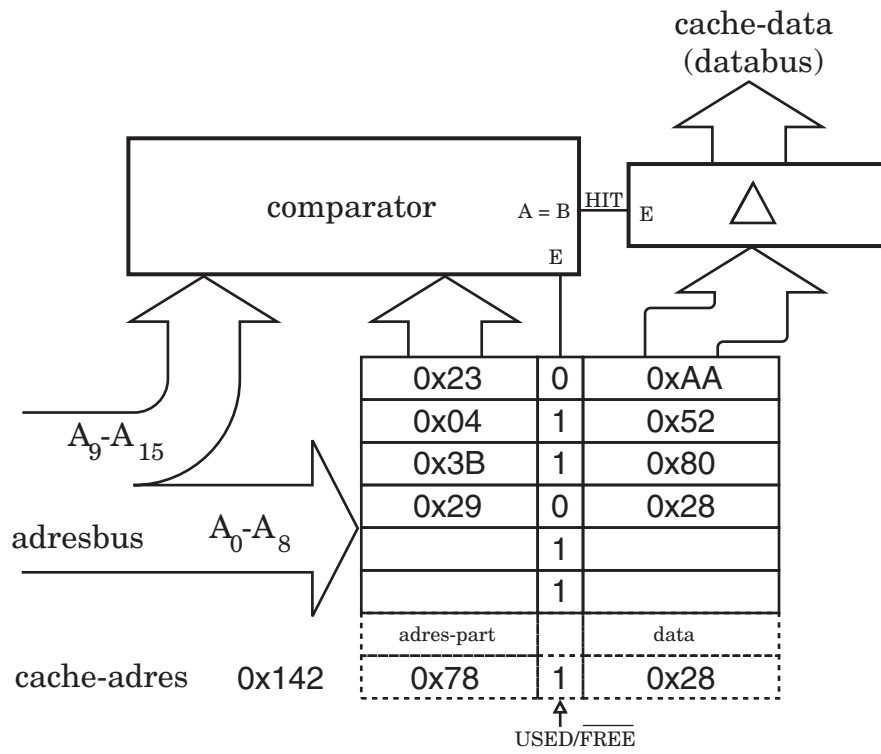
Figuur 11.5: Associatief geheugenwoord.

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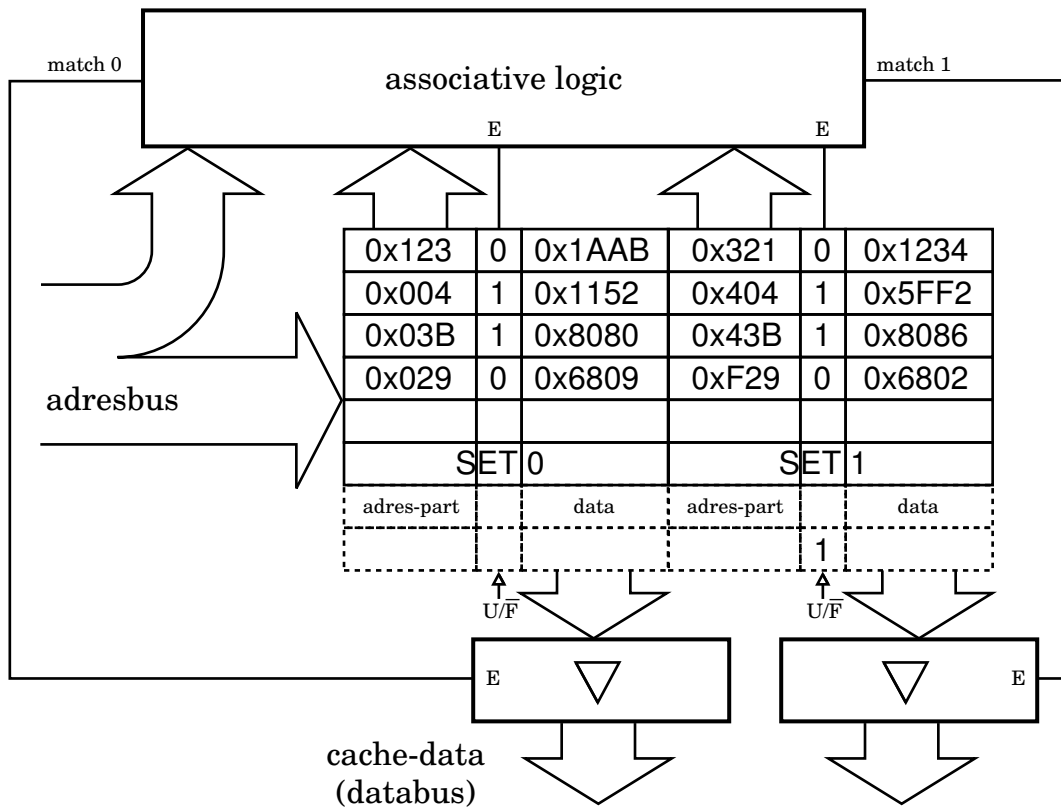
memory bits (adressen)	USED/ $\overline{\text{FREE}}$	TAG-bits (cache-data)
0x7FFF	0	0x00AA
0x034A	1	0xB752
0x03BB	1	0x8000
0x0299	0	0x2708
0x1000	1	0x7151
0x3055	1	0x2222

Figuur 11.6: Associatieve cache.

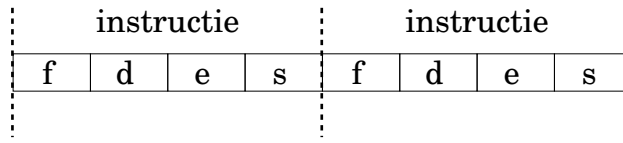
Computersystemen en embedded systemen (LvM)



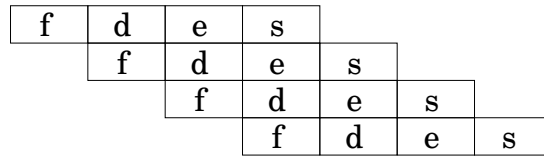
Figuur 11.7: Direct mapping cache.



Figuur 11.8: Set-associatieve cache.



Figuur 11.9: Normale instructieafhandeling.



Figuur 11.10: Pipeline.

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f	d	e	s	f	d	e	s
f	d	e	s	f	d	e	s

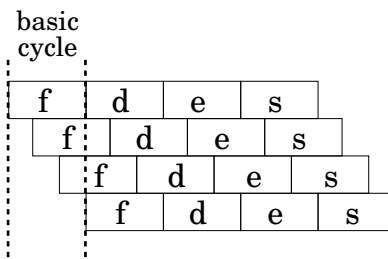
Figuur 11.11: Superscalaire instructieafhandeling.

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f	d	e	s		
f	d	e	s		
	f	d	e	s	
	f	d	e	s	
		f	d	e	s
		f	d	e	s

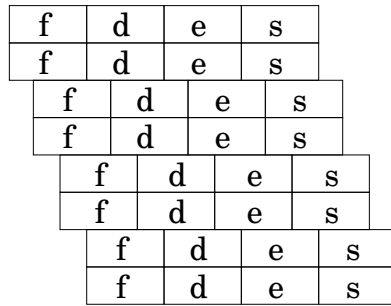
Figuur 11.12: Superscalaire architectuur plus pipelining.

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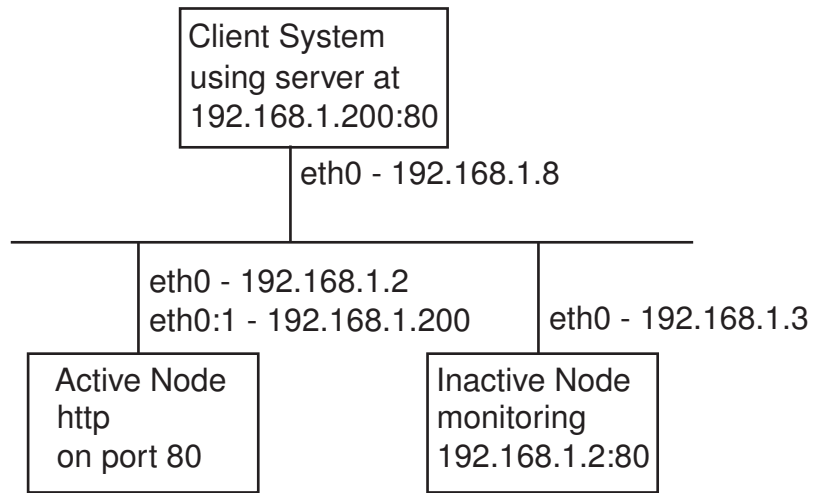
Figuur 11.13: Superpipeline.

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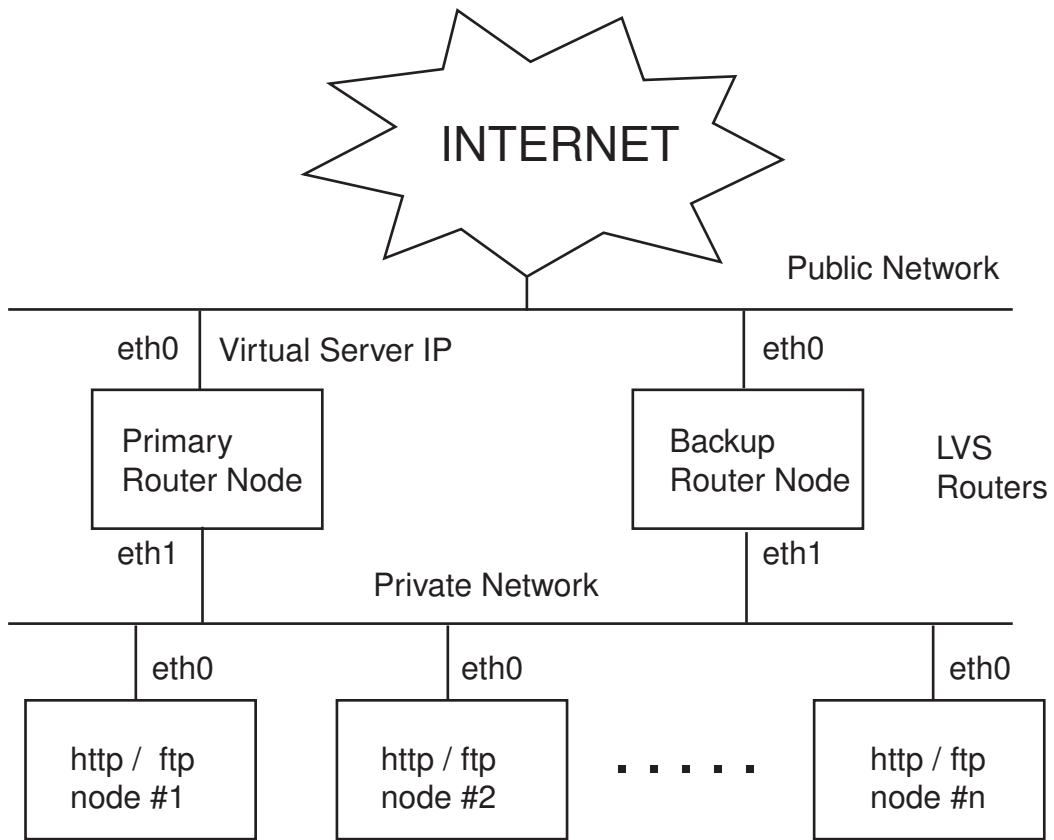
Figuur 11.14: Superscalaire architectuur met superpipelining.

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Figuur 11.15: Componenten van een fos.

Computersystemen en embedded systemen (LvM)



Figuur 11.16: Opbouw van een lvs.

Computersystemen en embedded systemen (LvM)